AdVirgo Mirror Suspensions

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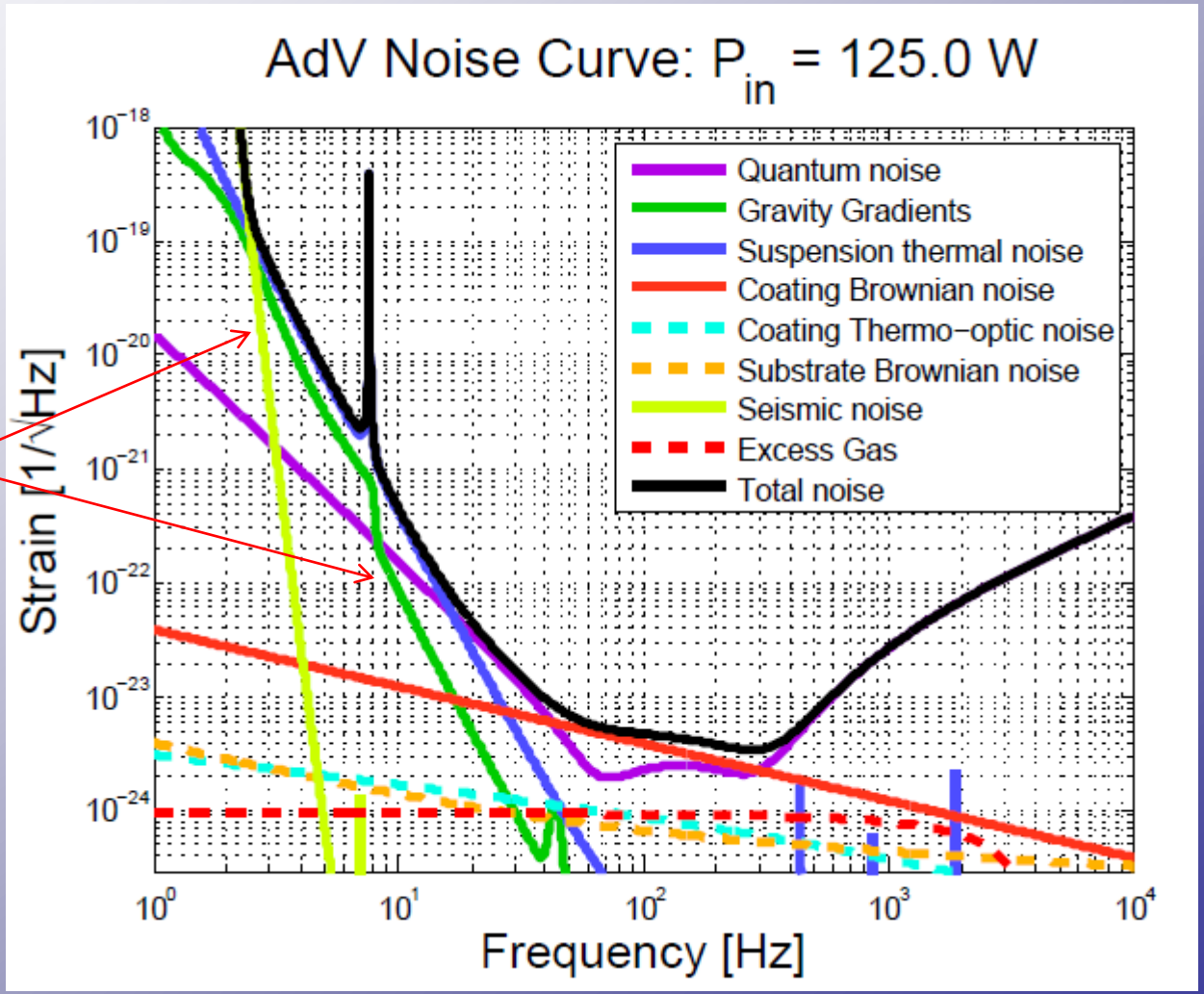
Outline

- Noise sources of GW interferometers
- The mirrors
- The Superattenuator (SA)
  - Mechanical design
  - Control system

AdVirgo
Baseline sensitivity curve

Newtonian and Seismic noise dominate at low frequency

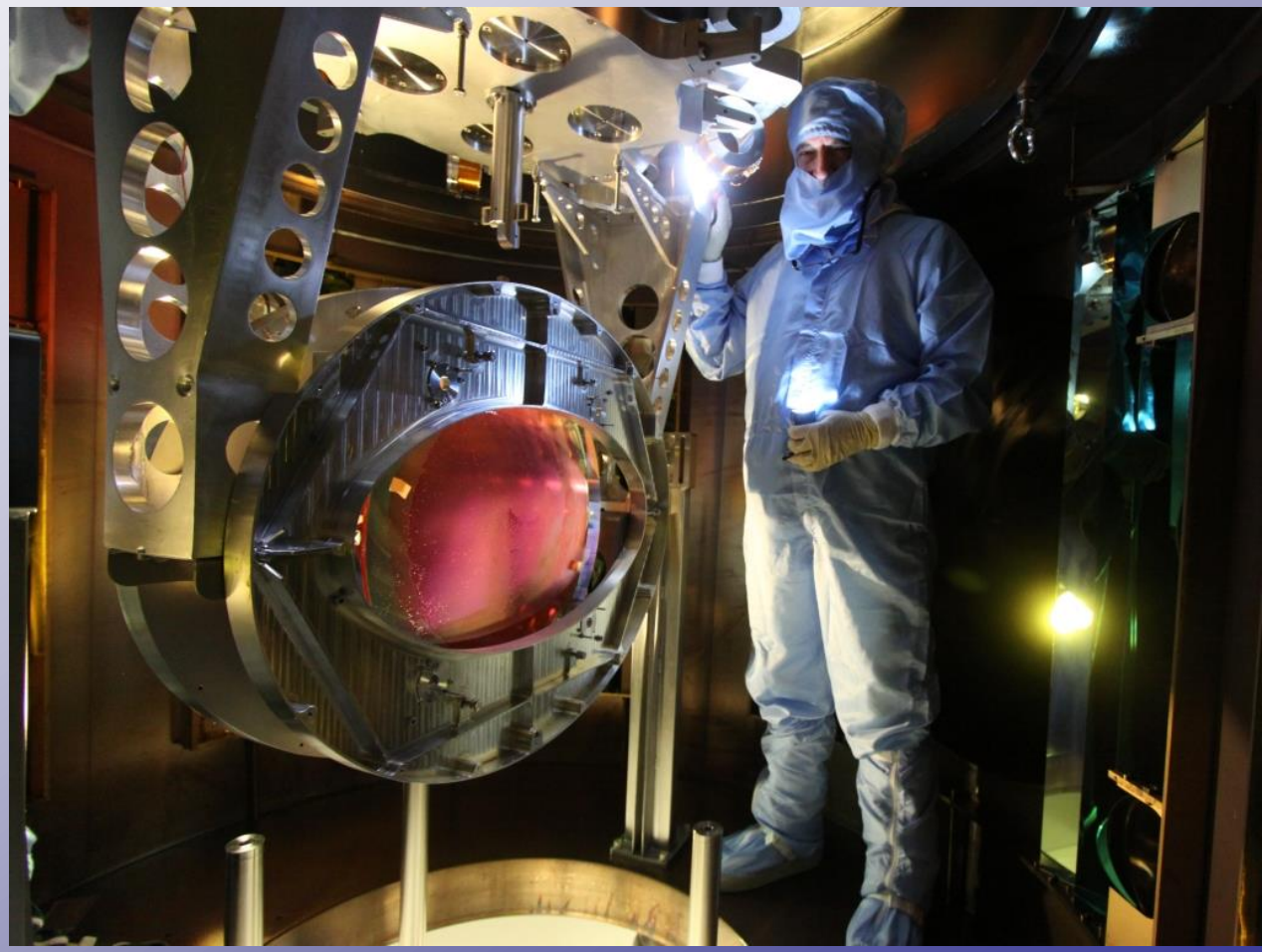


AdVirgo Mirrors

- Mirrors are made of Suprasil SiO_2, 350 mm of diameter, 200 mm wide, surface roughness $< 10^{-8}$ m.
- Coating is done using Ti doped Ta_2O_5
- Monolithic suspensions: made with extremely thin SiO2 fibers (400 µm of diameter) to suspend mirrors of about 42 kg.

AdVirgo Mirrors

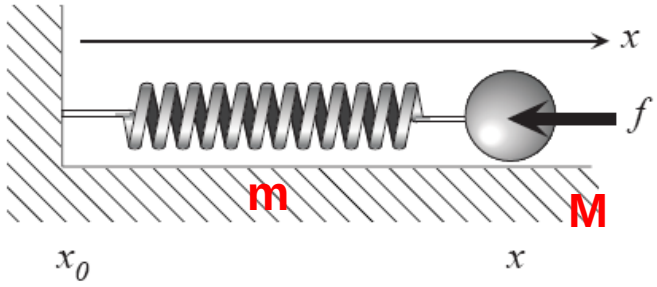
- **The first mirror of the ‘new generation’**
- 550 mm of diameter, 65 mm of width
- About 34 kg of total weight
- It’s the test mass supported by the Beam Splitter suspension



Introduction
Harmonic Oscillators as Mechanical filters

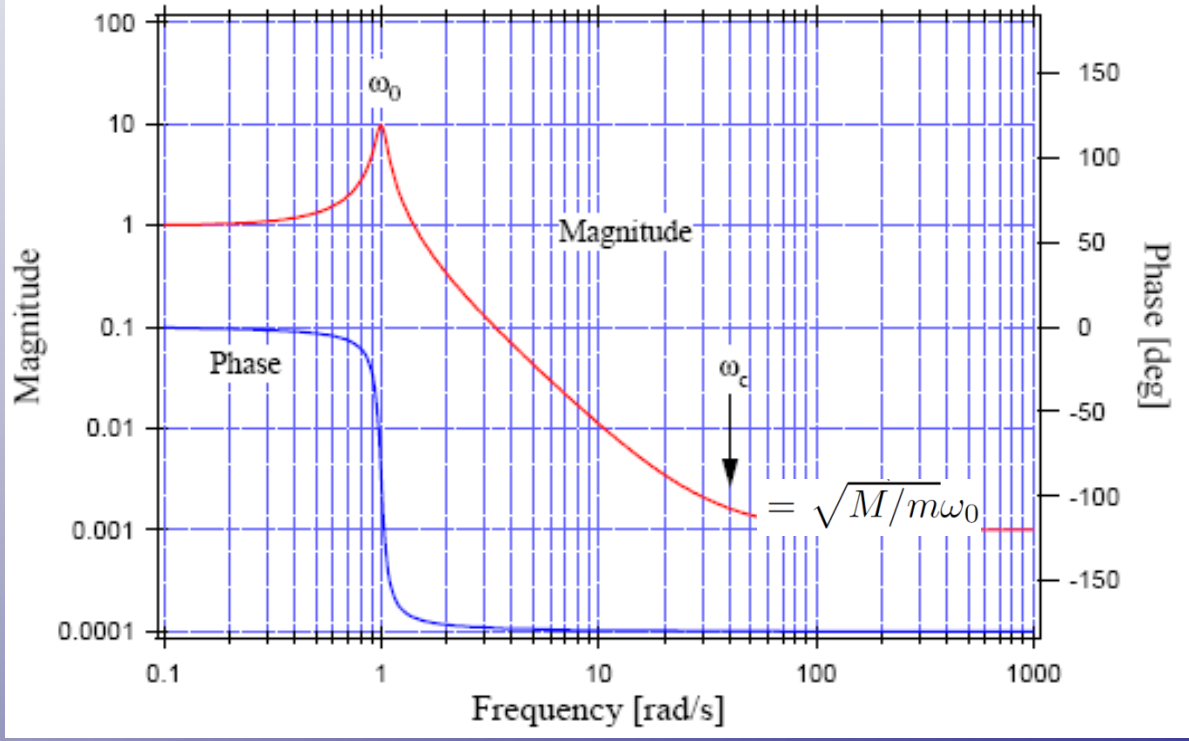
At frequencies higher than the oscillator resonance, the transfer function of an harmonic oscillator is equivalent to a second-order low pass filter.

Massive Spring

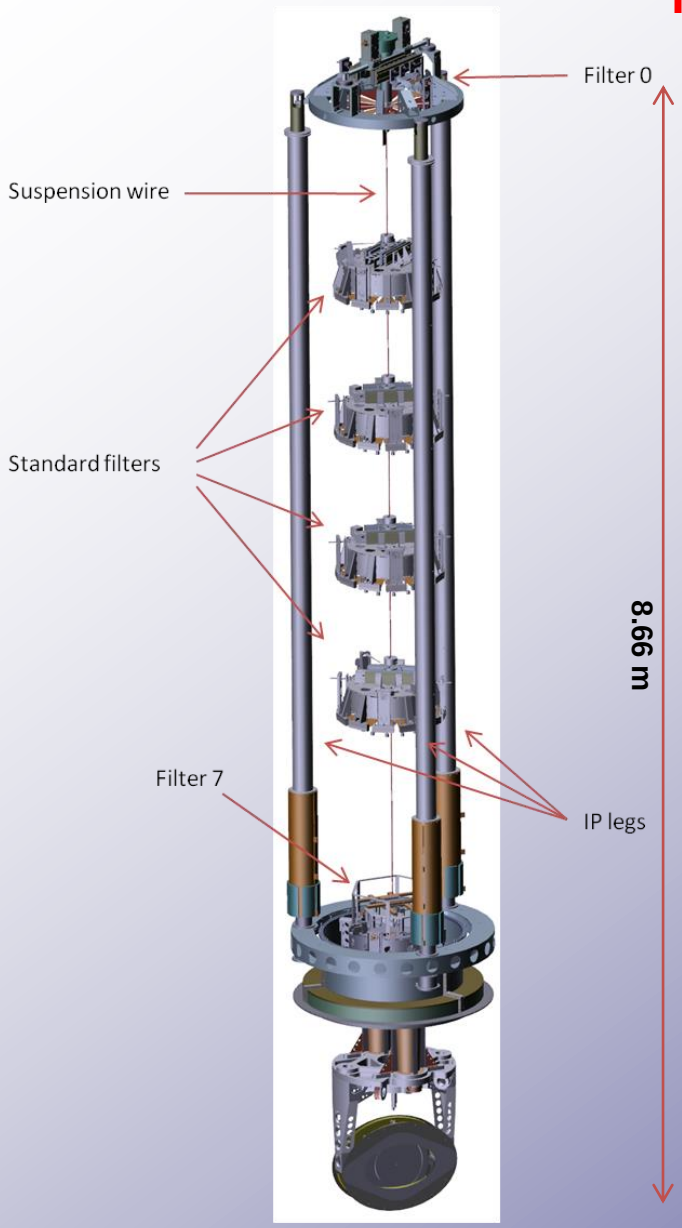


$$H_X = \frac{\omega_0^2(1+i\phi)+\frac{m}{M}\omega^2}{\omega_0^2(1+i\phi)-\omega^2+i\frac{\gamma}{M}\omega}$$

Transfer Function



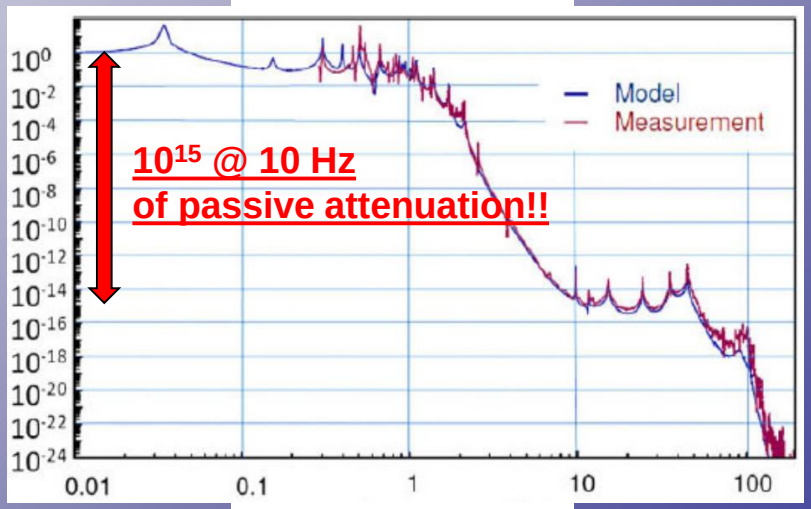
AdVirgo Superattenuator
The superattenuator (SA)



The AdVirgo superattenuator (SA) is a complex mechanical device capable of providing more than 10 orders of magnitude of passive seismic isolation in all six degrees of freedom above a few Hz

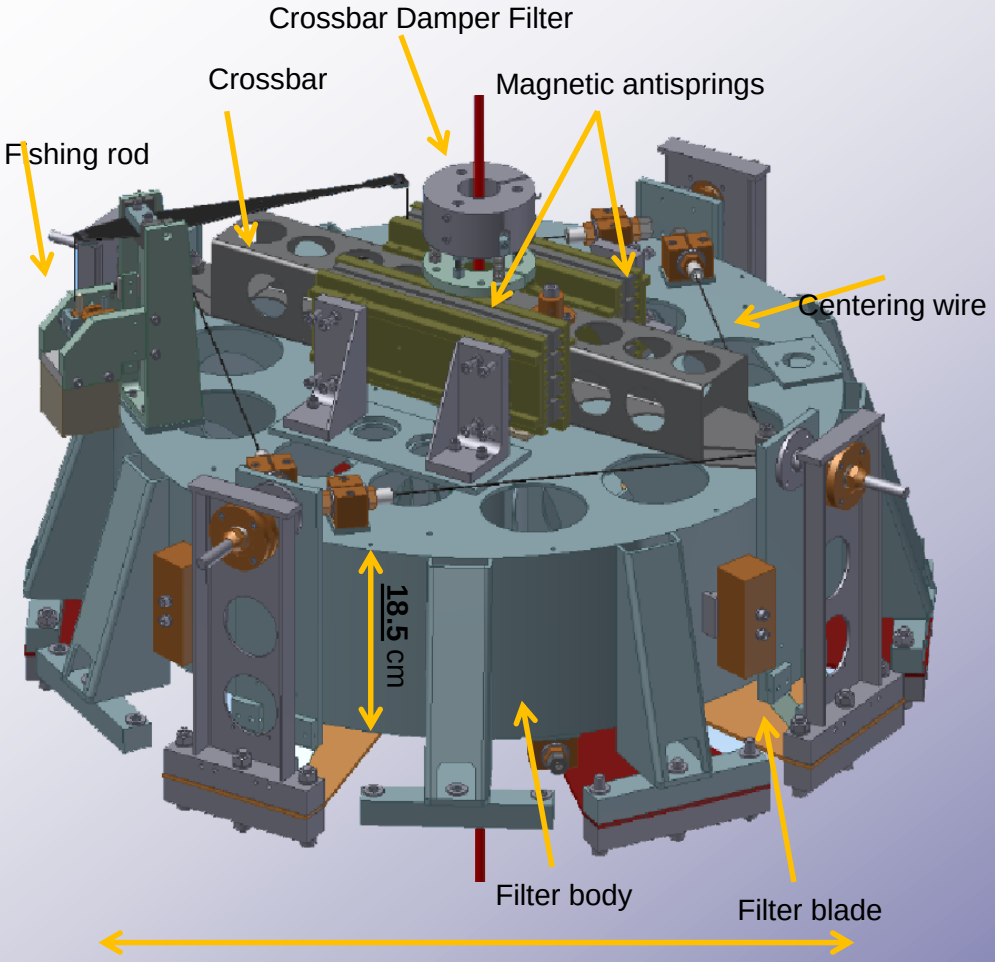
- The SA is a passive mechanical system constituted by a 5 stage pendulum supported by a 3-leg elastic pre-isolator called inverted pendulum (IP).
- All the normal mode resonance frequencies of the SA are kept below 2 Hz.
- The SA mechanical structure, consists of three fundamental parts: the inverted pendulum, the chain of standard filters, the payload.
- Mechanical design for AdVirgo is essentially the same of Virgo except for the payload.

Transfer function



AdVirgo Superattenuator

The Standard Filters

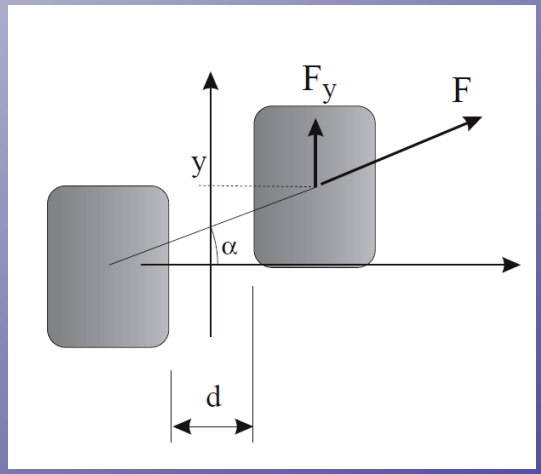


10^2 for $f > 2$ Hz of passive attenuation in both horizontal and vertical direction !!

The first four pendulum stages of the SA are denominated Standard Filters (SFs).

The SF is essentially a rigid steel cylinder supporting a set of maraging steel cantilevered triangular blades clamped along the outer surface of the filter body.

A magnetic anti-spring system, assembled on each filter, is designed
to reduce its fundamental vertical frequency from about 1.5 Hz down below 0.5 Hz.



Magnetic antispring working principle

AdVirgo Superattenuator
Control system

On long superattenuators (BS, NI, NE, WI, WE, PR, SR) are installed:

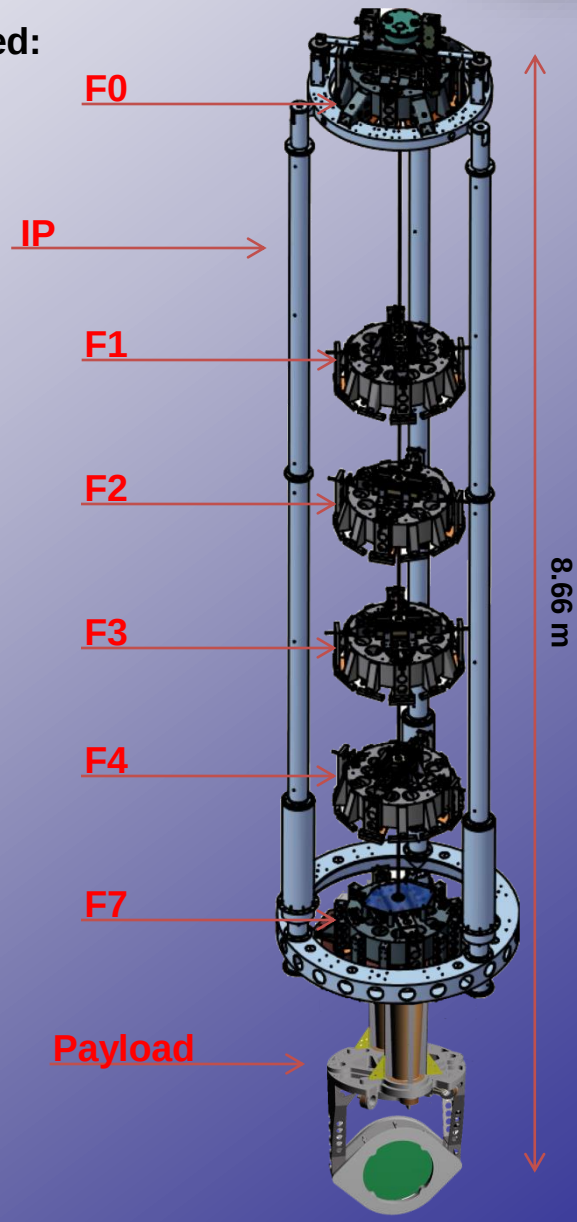
- **18 LVDTs** of 3 different types
  - 9 Vertical LVDTs (F0 – F7 Crossbar, Bottom Ring)
  - 3 F0 Horizontal LVDT
  - 6 F7 LVDTs

- **5 Accelerometers** of 2 different types installed on F0:
  - 3 Horizontal Accs
  - 2 Vertical Accs

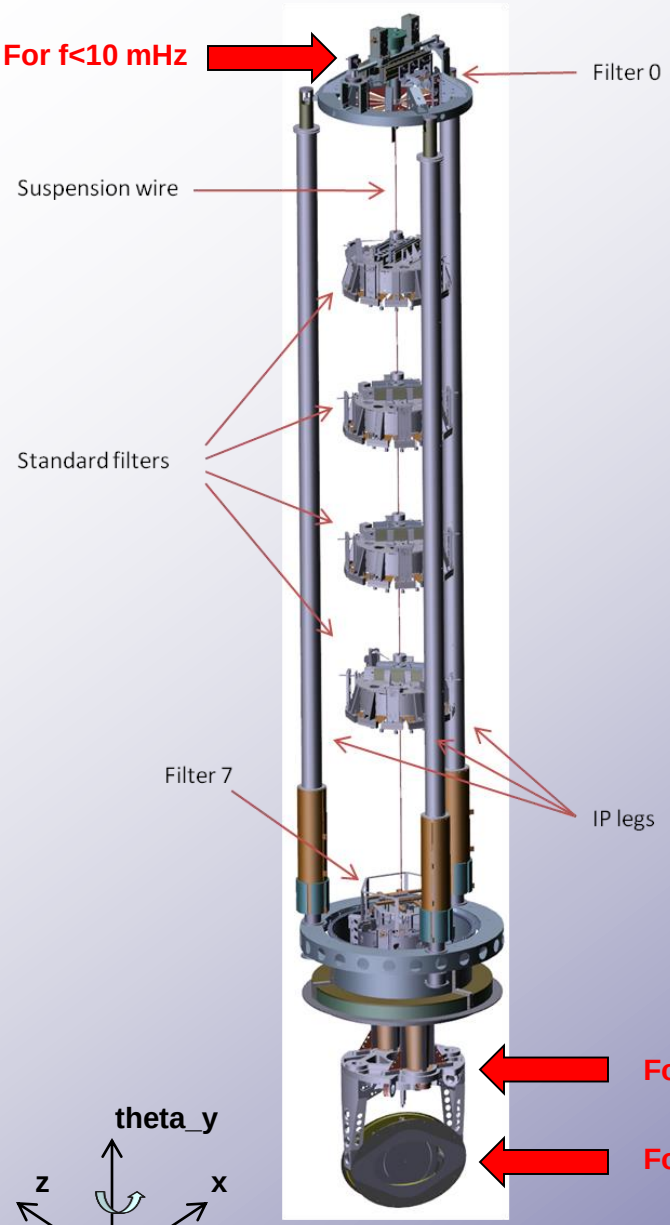
- **23 Coils** of 4 different types
  - 5 F0 Coils
  - 6 F7 Coils
  - 8 Marionette coils
  - 4 Mirror coils

- **3 Piezos** on bottom ring (**Not uset yet**)

- **21 Motors**
  - 1 Top screw F0 vertical motor
  - 3 F0 trolley motors
  - 6 Fishing rod motors
  - 2 Marionette motors
  - 4 F7 motors
  - 5 Accelerometer motors



AdVirgo Superattenuator
Control system



The control system has been designed using a hierarchical strategy regulated by the dynamic range of the actuators.

- 23 Coil Magnet Actuators in 3 points (actuation stages) of the SA:
- **Filter 0**:
Large displacements (hundreds of microns) for f<10 mHz.
- **Filter 7 + Marionette**:
Small payload displacements (1 micron) in the 10 mHz<f<1 Hz band.
- **Filter 7 + Mirror**:
Small residual mirror displacements (a few nm), for f>1 Hz.

- **>**20 Local Sensors
- Accelerometers
- 4 Displacements Sensors (LVDTs) on Filter 0
- 6 Displacements Sensors on Filter 0
- Optical Readout of Marionette and Mirror Position

- Digital Control system based on high-performance multicore DSPs.

- The total computing power in single precision available for the control of each SA and the processing of its signals will be 2.2 TFLOPs !!

AdVirgo Superattenuator
Control sytem hardware

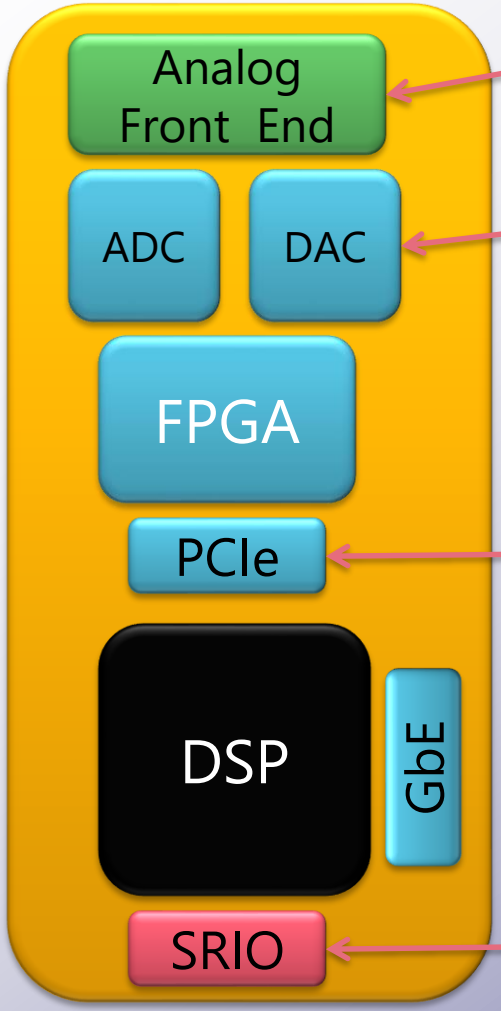
- **Electronics Design based on Texas Instruments DSP**
  - TMS320C6678
    - Eight TMS320C66x DSP Core Subsystems
    - 320 GMAC/160 GFLOP @ 1.25GHz
    - Four Lanes of SRIO 2.1 - 5 Gbaud Per Lane Full Duplex
    - Two Lanes PCIe Gen2 - 5 Gbaud Per Lane Full Duplex
    - Ethernet MAC Subsystem - Two SGMII Ports w/ 10/100/1000 Mbps operation
    - 64-Bit DDR3 Interface (DDR3-1600)

Computing power of a high-end GPU but extremely energy efficient and specifically designed for hard real-time applications

Platform		Effective Time to complete 1024 complex to complex FFT (single precision) μs	Power (Watts)	Energy per FFT (μJ)
GPU	nVidia Tesla C2070	0.16	225	36
GPU	nVidia Tesla C1060	0.3	188	56.4
GPP	Intel Xeon Core Duo @ 3 GHz	1.8	95	171
GPP	Intel Nehalam Quad Core @ 3.2 GHz	1.2	130	156
DSP	TI C6678 @ 1.2 GHz	0.86	10	8.6

AdVirgo Superattenuator

Control system hardware



10 Vpp, differential I/O

6ch ADC 24bit, up to 3.84 MSPS
6ch DAC 24bit, up to 640 kSPS

Analog and digital parts have been embedded in a single board.

2 lanes x Gen2 PCIe (up to 10 Gbps)

Gigabit Ethernet - Control

Up to 12 modules per crate

4 lanes x SRIO (up to 20 Gbps)

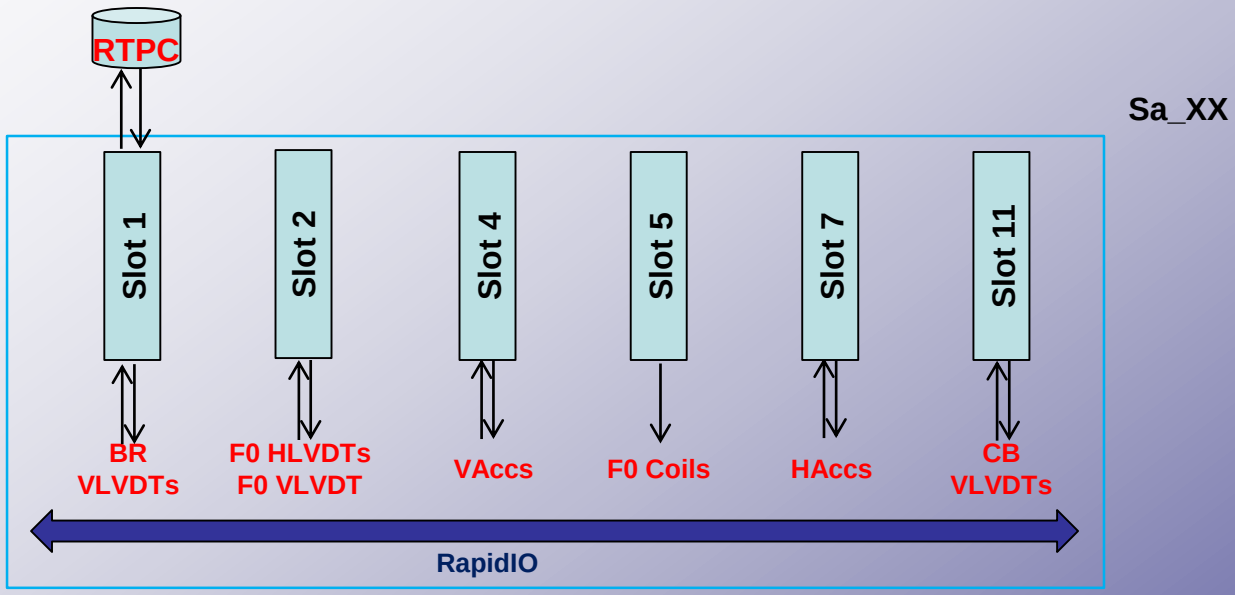
RapidIO Switch

Eth

100baseT - Management

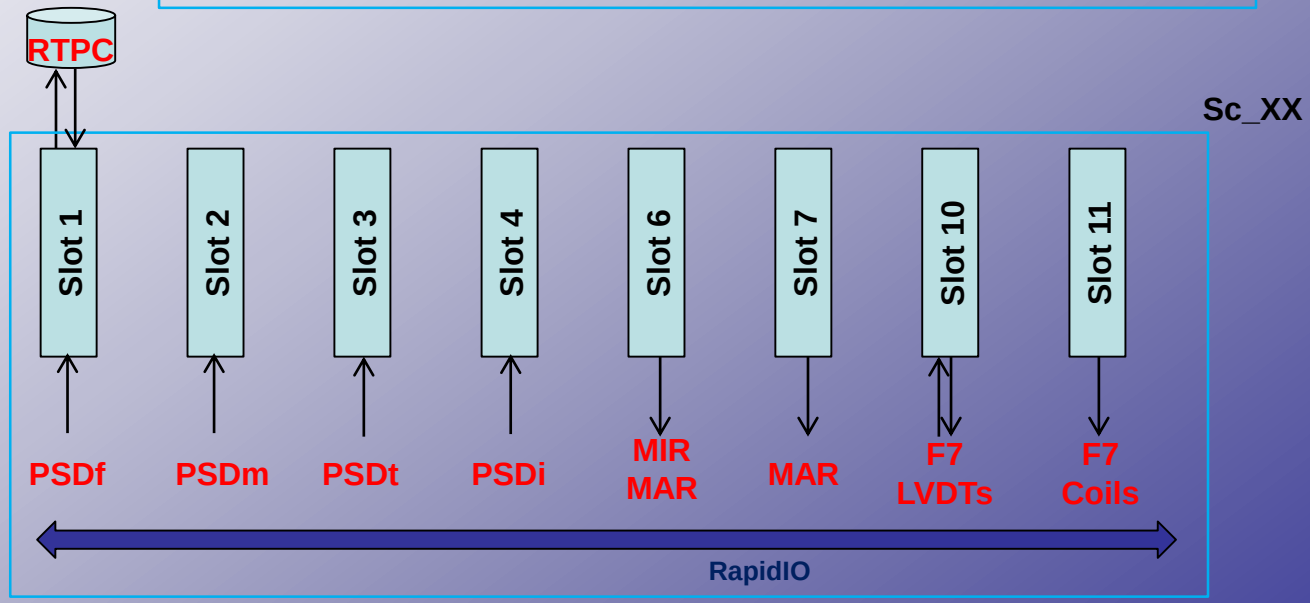
AdVirgo Superattenuator
Control system hardware

• A total of 14 boards, each one equipped with an 8-core TMS320C6678 DSP, are connected to each long suspension:



Total computing power of each SA :

> 2.2 TFLOPs !!



AdVirgo Superattenuator
Control system software

SA control is an extremely complex system:

- **131** DSP boards are installed on BPC, BS, IB, MC, PR, NI, NE, WI, WE, SR, OB
- **185** control code files are running at the same time on the DSP cores at 10 kHz (IP, F7, LC controls), 40 kHz (Global signals oversampling) and 320 kHz (Digital demodulation of sensors)

- All the DSP software (code, generated assembler and binaries) is archived in an SVN repo that can be browsed:
https://svn.ego-gw.it/svn/satsw/DSPCode_Adv/

O2 SOFTWARE MAP

SA	BOARD IP	CONNECTED DEVICES	SOFTWARE RUNNING (Core4, 10 kHz)	SOFTWARE RUNNING (Core1, 320 kHz)
BPC	172.16.2.104	PSD	/virgoDev/Sa/DSPCode_Adv/BPC/BPC_PSD	
BPC	172.16.2.141	PIEZO	/virgoDev/Sa/DSPCode_Adv/BPC/BPC_CD	
Sa_BS	172.16.2.62	BR LVDTs	/virgoDev/Sa/DSPCode_Adv/BS/LVDT/BS_MASTER	/virgoDev/Sa/DSPCode_Adv/BS/LVDT/BS_BR_LVDT_Demod
Sa_BS	172.16.2.53	F0 LVDTs	/virgoDev/Sa/DSPCode_Adv/BS/LVDT/BS_LVDT_HG_SRIO	/virgoDev/Sa/DSPCode_Adv/BS/LVDT/BS_LVDT_HG2
Sa_BS	172.16.2.32	F0 VAccs	/virgoDev/Sa/DSPCode_Adv/BS/Accs/BS_vAcc_LQG	/virgoDev/Sa/DSPCode_Adv/BS/Accs/BS_vAcc_Demod
Sa_BS	172.16.2.33	F0 Coils	/virgoDev/Sa/DSPCode_Adv/BS/InertialDamping/BS_ID_Diag	
Sa_BS	172.16.2.133	F0 HAccs	/virgoDev/Sa/DSPCode_Adv/BS/Accs/BS_Acc_LQG	/virgoDev/Sa/DSPCode_Adv/BS/Accs/BS_Acc_Demod
Sa_BS	172.16.2.52	F1-F7 VLVDTs	/virgoDev/Sa/DSPCode_Adv/BS/LVDT/BS_VLVDT_SRIO	/virgoDev/Sa/DSPCode_Adv/BS/LVDT/BS_VLVDT
Sc_BS	172.16.2.80	PSD	/virgoDev/Sa/DSPCode_Adv/BS/LC/BS_PSDf	
Sc_BS	172.16.2.108	PSD	/virgoDev/Sa/DSPCode_Adv/BS/LC/BS_PSDm	
Sc_BS	172.16.2.110	PSD	/virgoDev/Sa/DSPCode_Adv/BS/LC/BS_PSDt	
Sc_BS	172.16.2.84	PSD	/virgoDev/Sa/DSPCode_Adv/BS/LC/BS_PSDi	
Sc_BS	172.16.2.181	MIR, MAR Coils	/virgoDev/Sa/DSPCode_Adv/BS/LC/BS_Mir	
Sc_BS	172.16.2.179	MAR Coils	/virgoDev/Sa/DSPCode_Adv/BS/LC/BS_Mar	
Sc_BS	172.16.2.139	F7 LVDT	/virgoDev/Sa/DSPCode_Adv/BS/LVDT/BS_F7_LVDT	/virgoDev/Sa/DSPCode_Adv/BS/LVDT/BS_F7_LVDT_Demod
Sc_BS	172.16.2.120	F7 Coils	/virgoDev/Sa/DSPCode_Adv/BS/F7/BS_F7_CD	
Sa_IB	172.16.2.28	BR LVDTs	/virgoDev/Sa/DSPCode_Adv/IB/LVDT/IB_MASTER	/virgoDev/Sa/DSPCode_Adv/IB/LVDT/IB_BR_LVDT_Demod
Sa_IB	172.16.2.130	F0, F4, F7 LVDTs	/virgoDev/Sa/DSPCode_Adv/IB/LVDT/IB_LVDT	/virgoDev/Sa/DSPCode_Adv/IB/LVDT/IB_LVDT_Demod
Sa_IB	172.16.2.9	F0 VAccs	/virgoDev/Sa/DSPCode_Adv/IB/Accs/IB_vAcc_LQG	/virgoDev/Sa/DSPCode_Adv/IB/Accs/IB_vAcc_Demod
Sa_IB	172.16.2.121	F0 Coils	/virgoDev/Sa/DSPCode_Adv/IB/InertialDamping/IB_ID_Diag	
Sa_IB	172.16.2.23	F0 HAccs	/virgoDev/Sa/DSPCode_Adv/IB/Accs/IB_Acc_LQG	/virgoDev/Sa/DSPCode_Adv/IB/Accs/IB_Acc_Demod
Sc_IB	172.16.2.118	PSD	/virgoDev/Sa/DSPCode_Adv/IB/LC/IB_PSDf	
Sc_IB	172.16.2.86	PSD	/virgoDev/Sa/DSPCode_Adv/IB/LC/IB_PSDi	
Sc_IB	172.16.2.107	PSD	/virgoDev/Sa/DSPCode_Adv/IB/LC/IB_PSDt	
Sc_IB	172.16.2.173	MAR Coils	/virgoDev/Sa/DSPCode_Adv/IB/LC/IB_Mar1	
Sc_IB	172.16.2.174	MAR Coils	/virgoDev/Sa/DSPCode_Adv/IB/LC/IB_Mar2	
Sa_MC	172.16.2.128	BR LVDTs	/virgoDev/Sa/DSPCode_Adv/MC/LVDT/MC_MASTER	/virgoDev/Sa/DSPCode_Adv/MC/LVDT/MC_BR_LVDT_Demod
Sa_MC	172.16.2.51	F0, F4, F7 LVDTs	/virgoDev/Sa/DSPCode_Adv/MC/LVDT/MC_LVDT	/virgoDev/Sa/DSPCode_Adv/MC/LVDT/MC_LVDT_Demod
Sa_MC	172.16.2.158	F0 VAccs	/virgoDev/Sa/DSPCode_Adv/MC/Accs/MC_vAcc_LQG	/virgoDev/Sa/DSPCode_Adv/MC/Accs/MC_vAcc_Demod
Sa_MC	172.16.2.103	F0 Coils	/virgoDev/Sa/DSPCode_Adv/MC/InertialDamping/MC_ID_Diag	
Sa_MC	172.16.2.14	F0 HAccs	/virgoDev/Sa/DSPCode_Adv/MC/Accs/MC_Acc_LQG	/virgoDev/Sa/DSPCode_Adv/MC/Accs/MC_Acc_Demod
Sa_MC	172.16.2.150	PIEZO	/virgoDev/Sa/DSPCode_Adv/MC/Tilt/Piezo_Test	
Sc_MC	172.16.2.101	PSD	/virgoDev/Sa/DSPCode_Adv/MC/LC/MC_PSDf	
Sc_MC	172.16.2.168	PSD	/virgoDev/Sa/DSPCode_Adv/MC/LC/MC_PSDi	
Sc_MC	172.16.2.88	PSD	/virgoDev/Sa/DSPCode_Adv/MC/LC/MC_PSDTf	
Sc_MC	172.16.2.109	PSD	/virgoDev/Sa/DSPCode_Adv/MC/LC/MC_PSDTi	
Sc_MC	172.16.2.171	MAR Coils	/virgoDev/Sa/DSPCode_Adv/MC/LC/MC_Mar1	
Sc_MC	172.16.2.172	MAR Coils	/virgoDev/Sa/DSPCode_Adv/MC/LC/MC_Mar2	
Sc_MC	172.16.2.176	MIR Coils	/virgoDev/Sa/DSPCode_Adv/MC/LC/MC_Mir	
Sa_NE	172.16.2.37	BR LVDTs	/virgoDev/Sa/DSPCode_Adv/NE/LVDT/NE_MASTER	/virgoDev/Sa/DSPCode_Adv/NE/LVDT/NE_BR_LVDT_Demod
Sa_NE	172.16.2.40	F0 LVDTs	/virgoDev/Sa/DSPCode_Adv/NE/LVDT/NE_LVDT	/virgoDev/Sa/DSPCode_Adv/NE/LVDT/NE_LVDT_Demod

Thank you for your attention!!