New DSP-based Control System for Advanced Virgo+ Phase II Upgrade

Hardware and firmware upgrades. Introducing in-system configuration capabilities for major flexibility.

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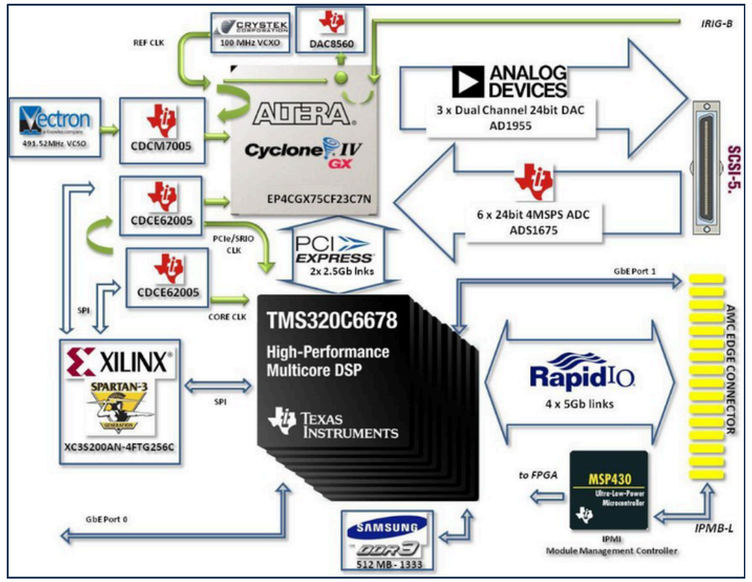
Current Hardware system

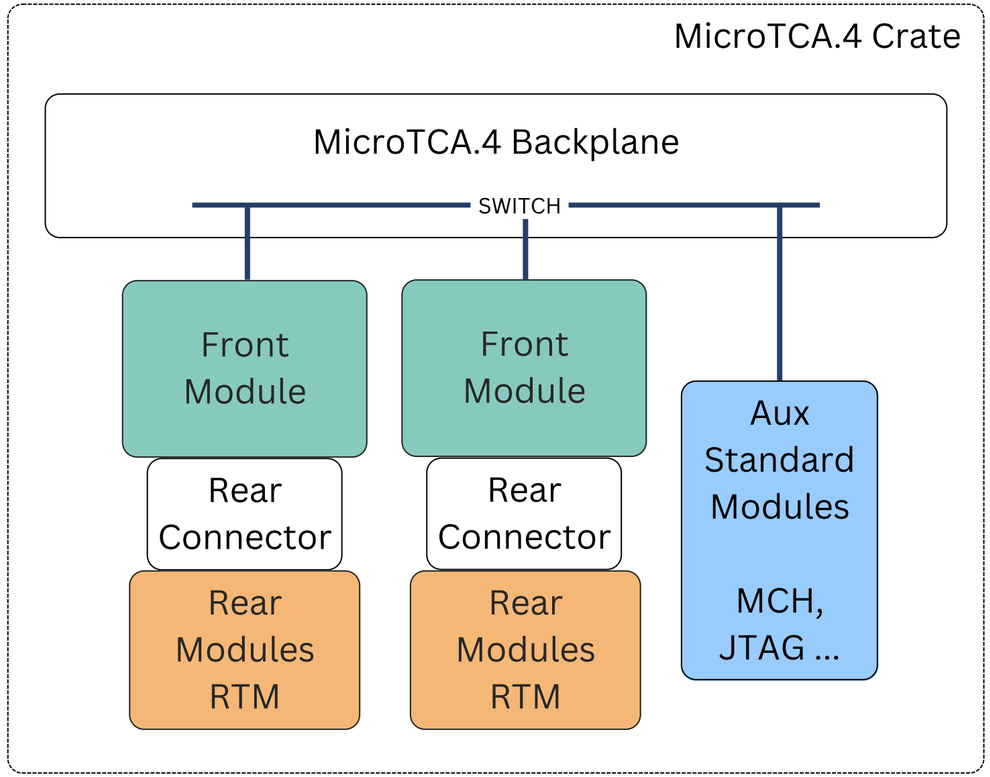
Currently, the SuperAttenuator control system is based on a customized MTCA-based architecture featuring a **single type custom board (UDSPT boards)**.

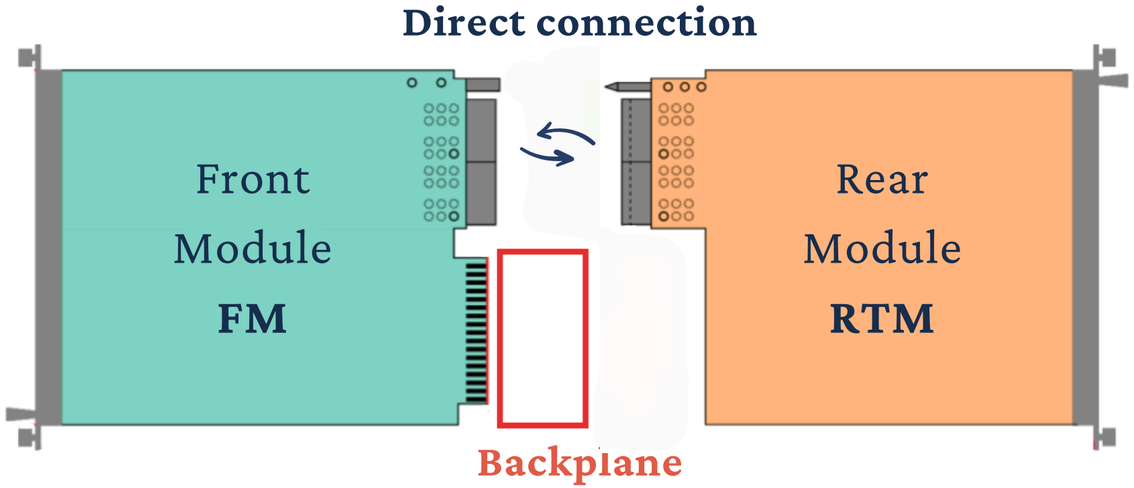


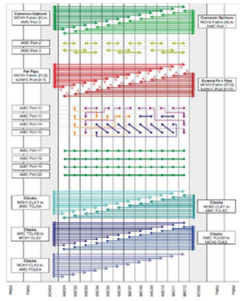
- **8 core DSP** TMS320C6678 (~20 GFLOPS/core)
- **6ch DAC** (24bit 320 kSPS)
- **6ch ADC** (24bit, 3.84MSPS)
- **FPGAs** for board configuration and signals data exchange (DSP <--> AD/DA, Timing, DAQ).

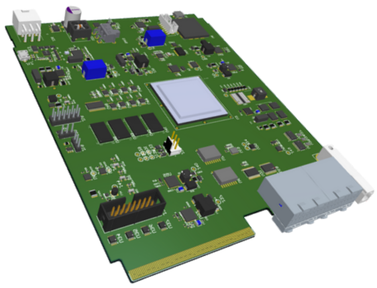
New Hardware System - 1

The new MPC control system will be based on MTCA.4 standard architecture featuring two different type of modules with different custom implementations (currently 1xFM, 2xRTM).





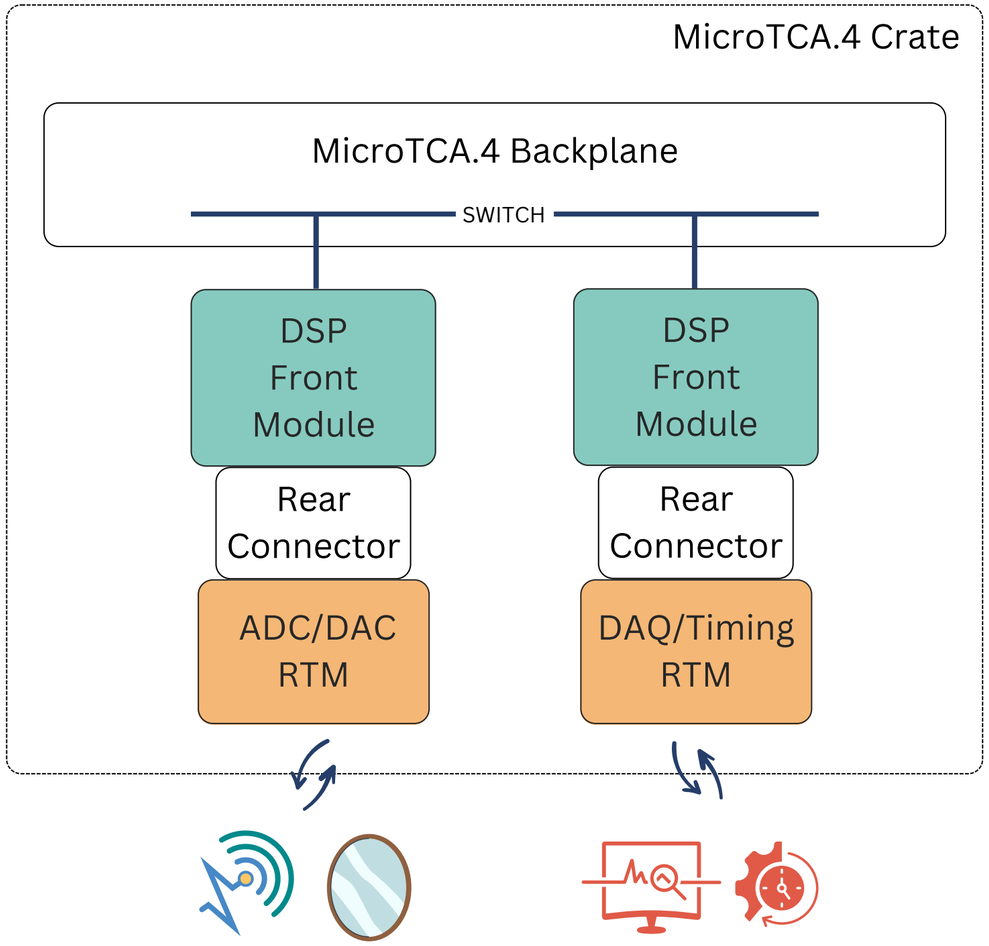




New Hardware System - 2

Current UDSPT board electronics will be split into different modules to increase system flexibility.
Three modules are today under development:

1. Front Module with DSP based electronics for data processing (FM-DSP).
2. RTM with Low-Noise data converters and front-end electronics (RTM-LDC).
3. RTM interfacing with other subsystems such as DAQ, Timing (RTM-TIM).



DSP Front Module

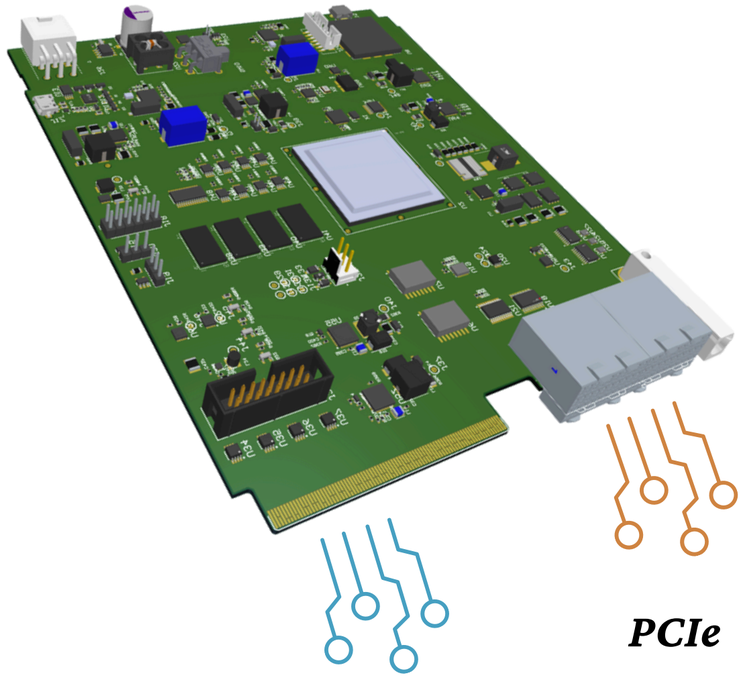
DSP front modules will mount a slightly different version of the Texas Instruments SoC (System on a Chip) used today.

66AK2H14 device features and advancements respect to current one:

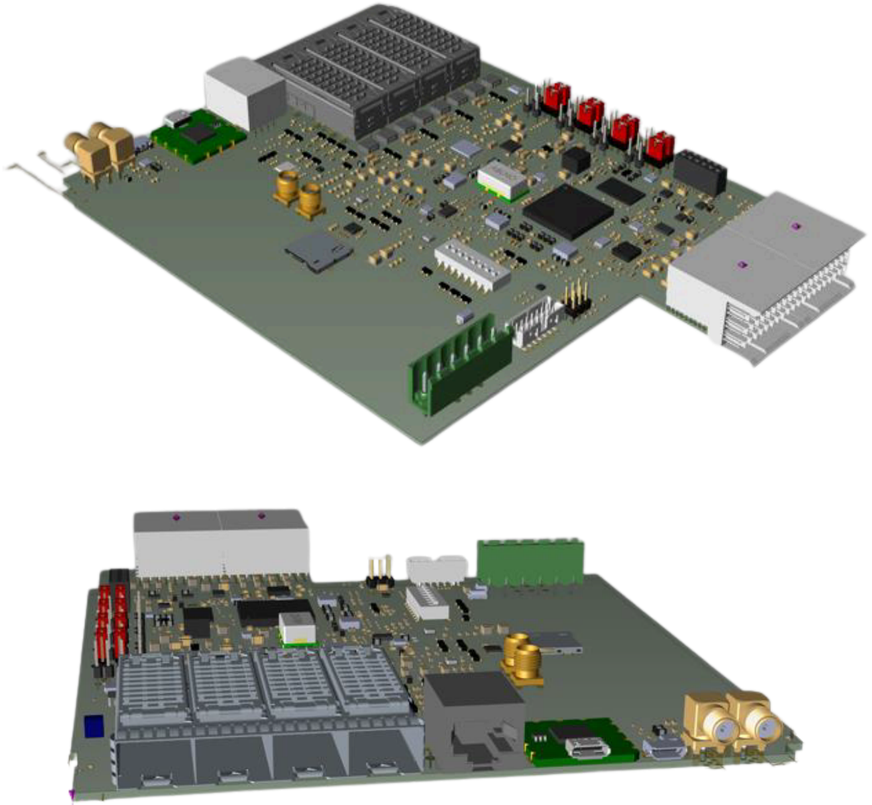
- Same powerful **x8 TMS320C66x DSP cores**.
- Same standard interfaces used for data exchange with other DSPs and ADC/DACs (**Serial RapidIO and PCIe**).

  ↳ Fully compatible with control algorithms running today.

- [PLUS] **x4** additional **ARM cores** (Better support for standard OS and software tools).
- [PLUS] 10Gb/s Ethernet interface.



DAQ/Timing Rear Transition Module



DAQ/Timing RTM is under development @ **INFN Bologna.**

Based on Artix Ultrascale+ FPGA devices.

Module's functionalities:

- Interface with Data acquisition system and global control.
- Interface with Virgo timing system and provide synchronized reference to a certain number of modules in the crate.

Support from **LAPP** for firmware development.

AD/DA Rear Transition Module

This module will host **data conversion devices and related front-end electronics** to interface with different types of sensors and actuators.

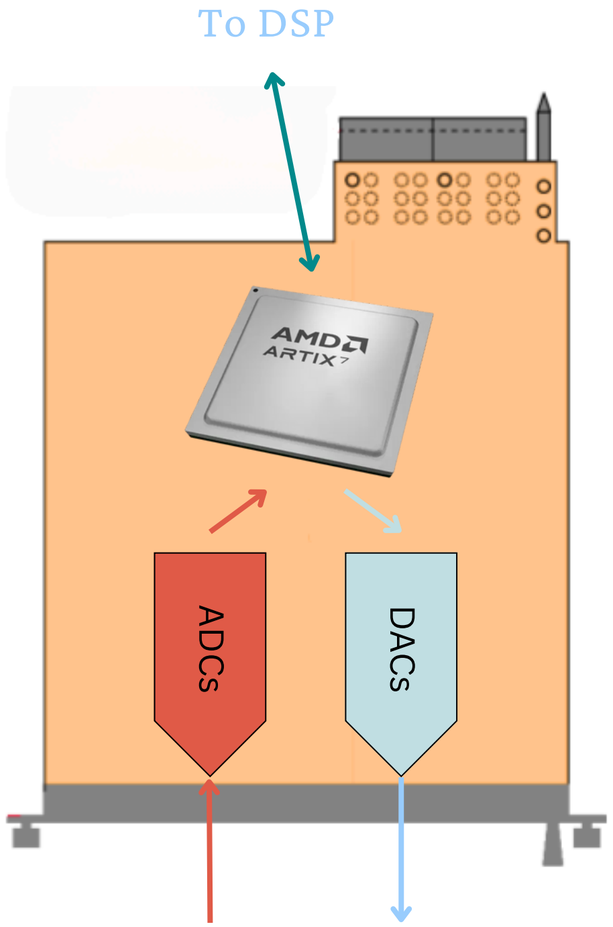
It will mount the same 24-bit converters used today (at least in first prototypes):

- **6 DAC channels** (24bit 320 kSPS)
- **6 ADC channels** (24bit, 3.84MSPS)

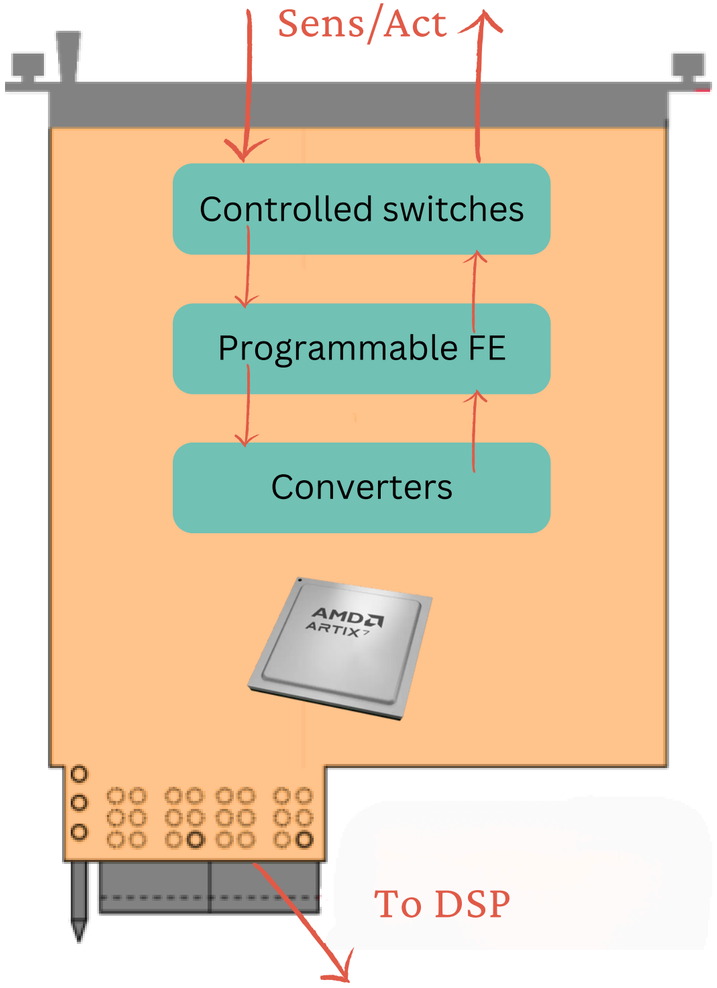
It will feature **Artix-7 FPGA devices** to implement board management, data pre-processing and routing from converters to DSPs and vice versa.

The new HW implementation will try to improve current board performances (spotted minor changes that can help advancing noise and stability).

Major change : SW configurable in terms of AC/DC coupling for input and output, Voltage/Current operation and signals ranges.



Firmware Development

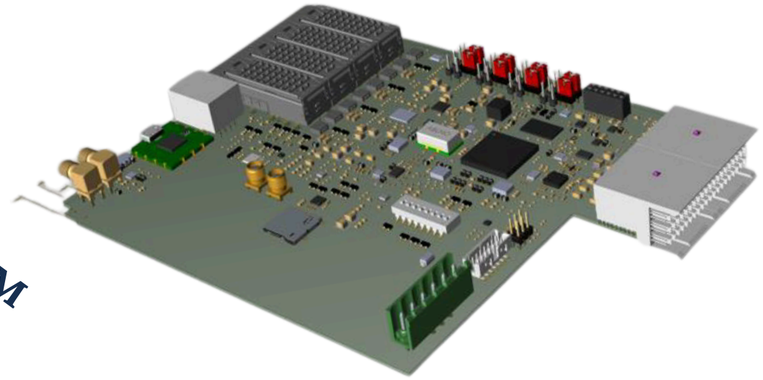


While the hardware architecture is changing significantly, there's also a lot of **firmware** work ahead.
We'll be able to re-use many existing firmware modules, but for the new AD/DA RTM and DAQ/Timing RTM, we still have significant developments to tackle:

- **Adapt designs** as we switch from **Altera to Xilinx** tool-chains.
- **Manage modular interconnections** across different boards.
- Support for **in-system FPGA reconfiguration**.

AD/DA RTM

DAQ TIMING RTM

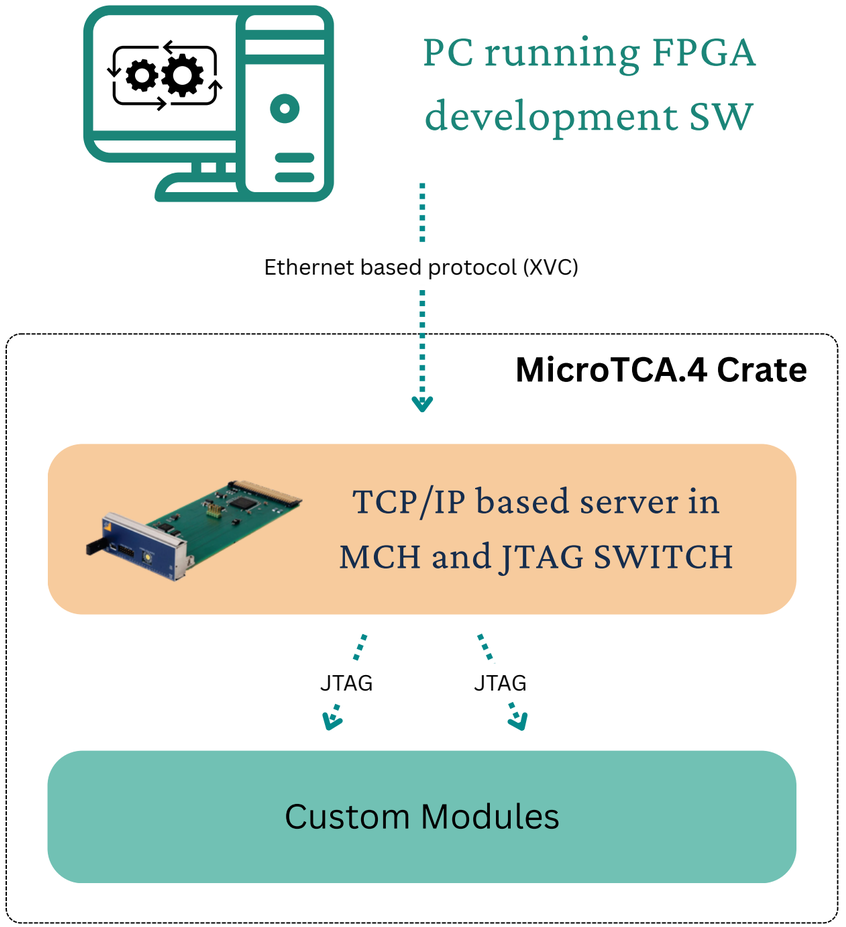


In-System Configuration - 1

Maybe the **major change** in the new real-time control system respect to the current one is the **In-System configuration capability**.

Currently it is not possible to reconfigure FPGAs firmware on the UDSPT board from remote → Manual intervention is required.

The new system will instead have this feature using **standard protocols and devices** to implement reconfiguration via **JTAG** from a remote controller.



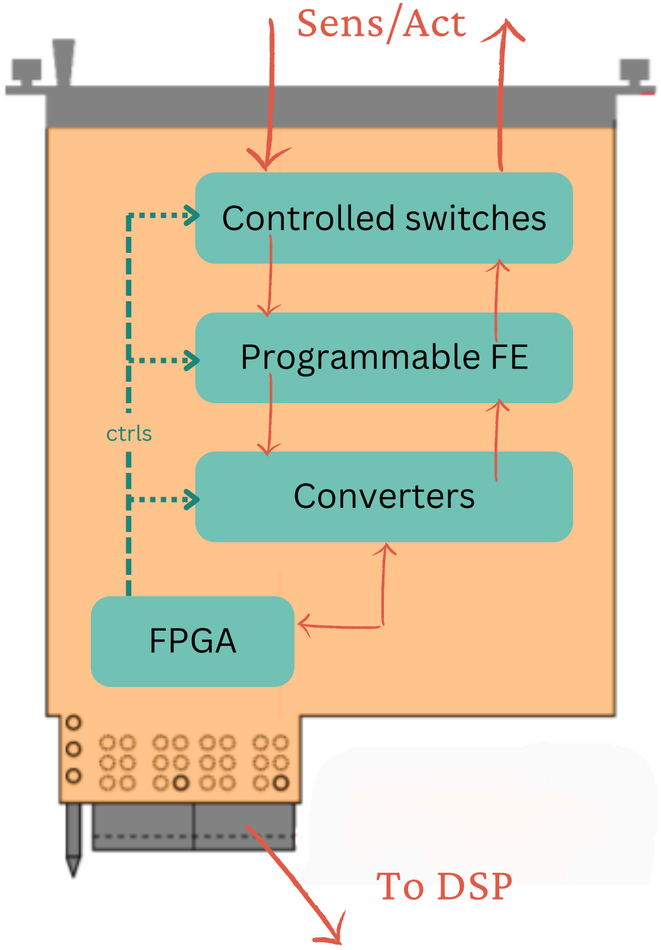
In-System Configuration - 2

AD/DA module use case

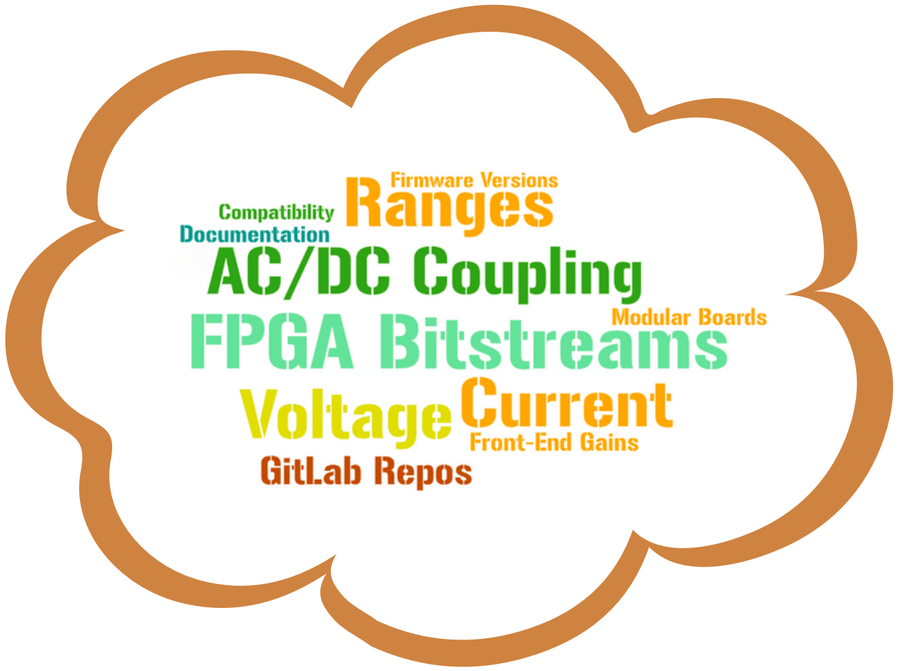
In the current UDSPT boards, hardware settings like **AC/DC coupling**, **voltage/current modes**, and **front-end gains** are fixed and require manual changes (e.g. soldering components). There are even multiple board versions differing in output **power delivery** for actuators.

With the new hardware, these settings will become software-driven.

Combined with the modular hardware approach, this should deliver significant flexibility improvements.



Software Layer - Flexibility Comes at a Price



In-system configuration option brings for sure **flexibility**, but it also add **complexity**. To fully benefit from new hardware we need:

- to **develop new software modules** to be able to operate and manage these changes.
- a **robust strategy** to handle:
  - **FPGA bitstreams** and versions.
  - **Hardware settings** (e.g. front-end gains, ranges, coupling modes).
  - **Compatibility** between hardware and sensors/actuators connected.

We're planning to adopt **GitLab** for firmware and software repositories, HW description files, System-level configurations. This should help us keep development organized, collaborative, and traceable.

Conclusions and open discussion

- The new MPC control system hardware offers more flexibility and modularity
- In-system configuration is a big step forward - but also demands new firmware and software tools.
- Open points for discussion :
  - How to best organize, store and track configurations ?
  - Which user-friendly tools should be developed for managing HW/FW configurations ?

Every input is really welcome !!

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